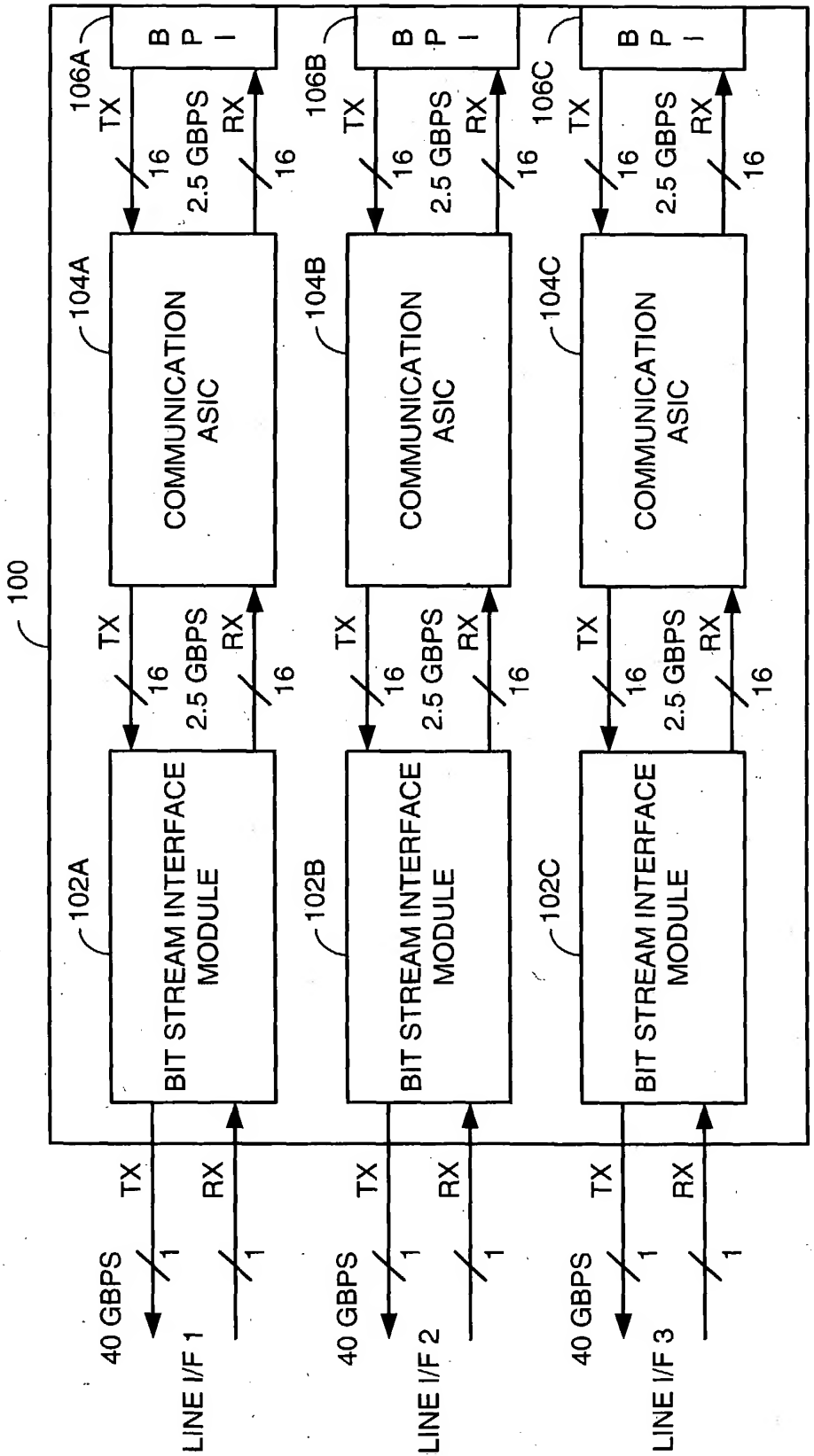

100
102A
BIT STREAM INTERFACE MODULE
102B
BIT STREAM INTERFACE MODULE
102C
BIT STREAM INTERFACE MODULE
104A
COMMUNICATION ASIC
104B
COMMUNICATION ASIC
104C
COMMUNICATION ASIC
106A
BPI
106B
BPI
106C
BPI
TX
RX
16
2.5 GBPS
40 GBPS
1
LINE I/F 1
LINE I/F 2
LINE I/F 3

FIG. 1

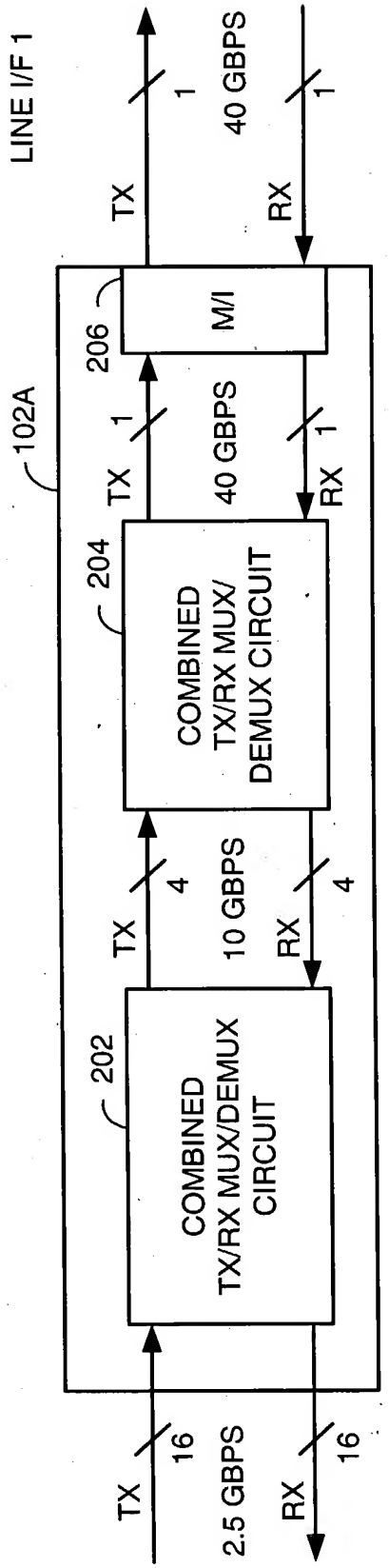

LINE I/F 1
102A
TX
16
2.5 GBPS
RX
16
202
COMBINED TX/RX MUX/DEMUX CIRCUIT
TX
4
10 GBPS
RX
4
204
COMBINED TX/RX MUX/ DEMUX CIRCUIT
TX
1
40 GBPS
RX
1
206
M/I
TX
1
40 GBPS
RX
1

FIG. 2A

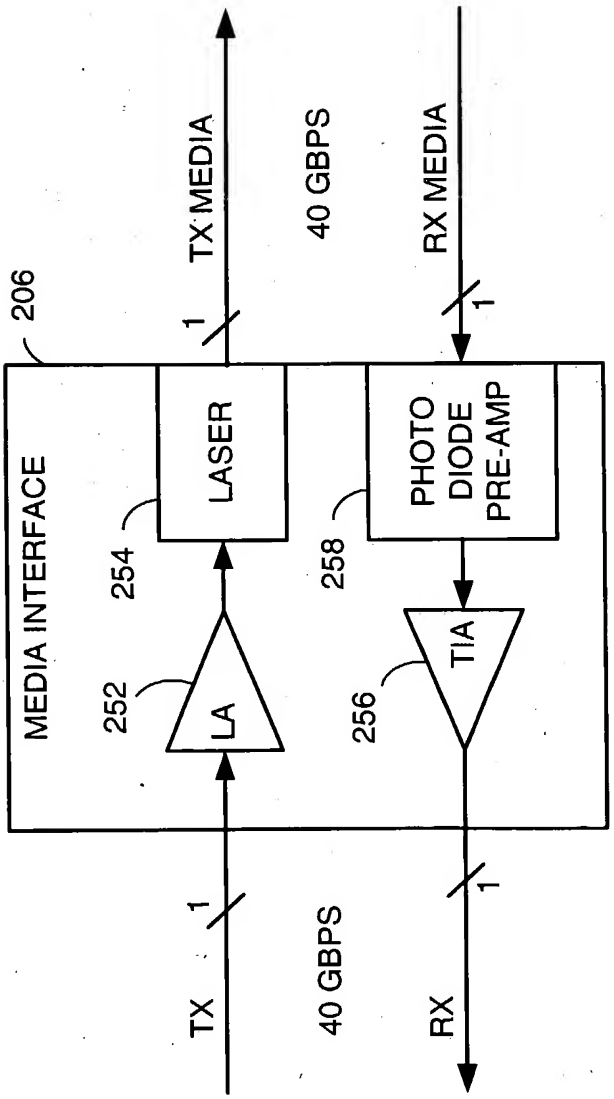

206
MEDIA INTERFACE
LASER
254
LA
252
PHOTO DIODE PRE-AMP
258
TIA
256
TX MEDIA
1
40 GBPS
RX MEDIA
1
TX
1
40 GBPS
RX
1

FIG. 2B

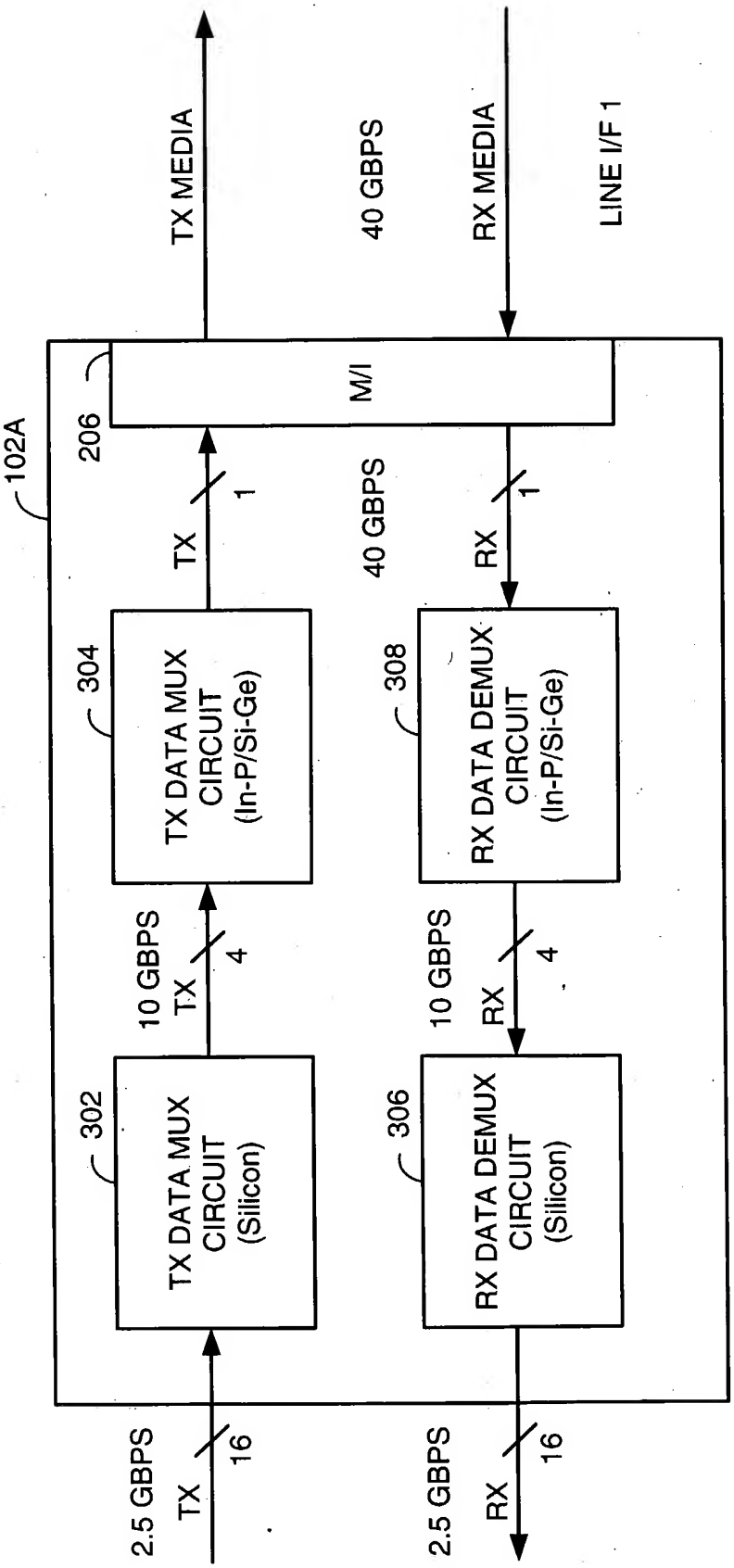

TX MEDIA
40 GBPS
RX MEDIA
LINE I/F 1
102A
206
M/I
TX
1
40 GBPS
RX
1
304
TX DATA MUX CIRCUIT (In-P/Si-Ge)
308
RX DATA DEMUX CIRCUIT (In-P/Si-Ge)
10 GBPS
TX
4
10 GBPS
RX
4
302
TX DATA MUX CIRCUIT (Silicon)
306
RX DATA DEMUX CIRCUIT (Silicon)
2.5 GBPS
TX
16
2.5 GBPS
RX
16

FIG. 3

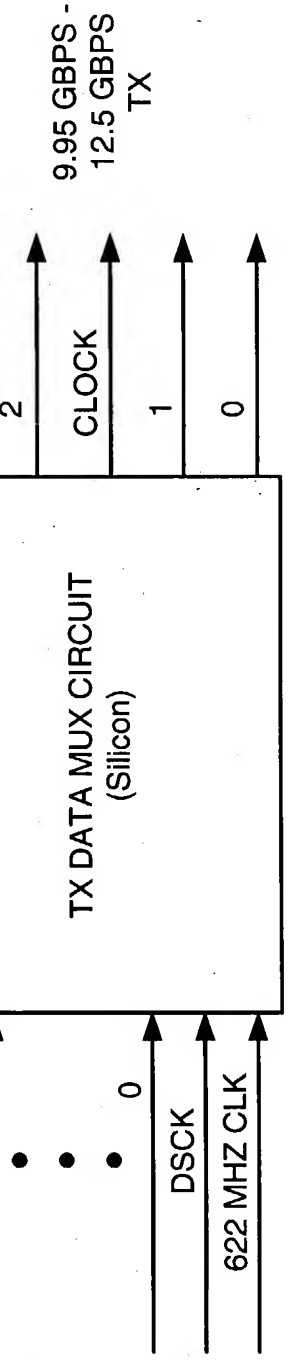

2.5 GBPS - 3.125 GBPS TX
15
14
0
DSCK
622 MHZ CLK
302
TX DATA MUX CIRCUIT
(Silicon)
3
2
CLOCK
1
0
9.95 GBPS - 12.5 GBPS TX

FIG. 4A

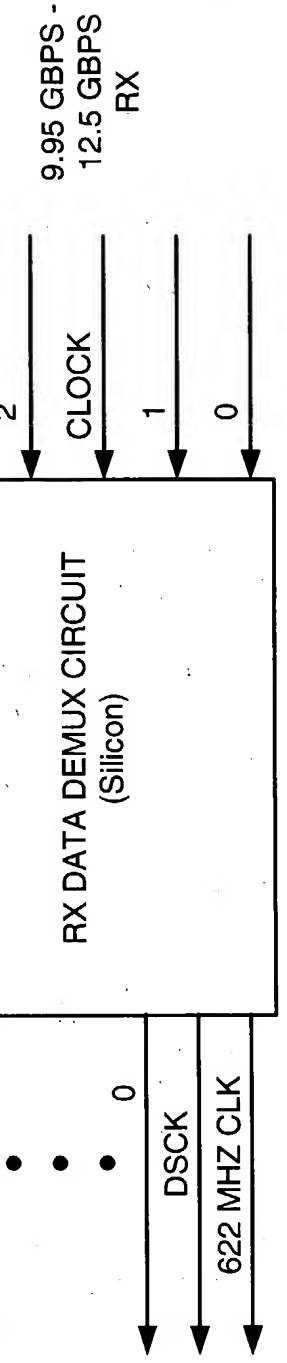

2.5 GBPS - 3.125 GBPS RX
15
14
0
DSCK
622 MHZ CLK
306
RX DATA DEMUX CIRCUIT
(Silicon)
3
2
CLOCK
1
0
9.95 GBPS - 12.5 GBPS RX

FIG. 4B

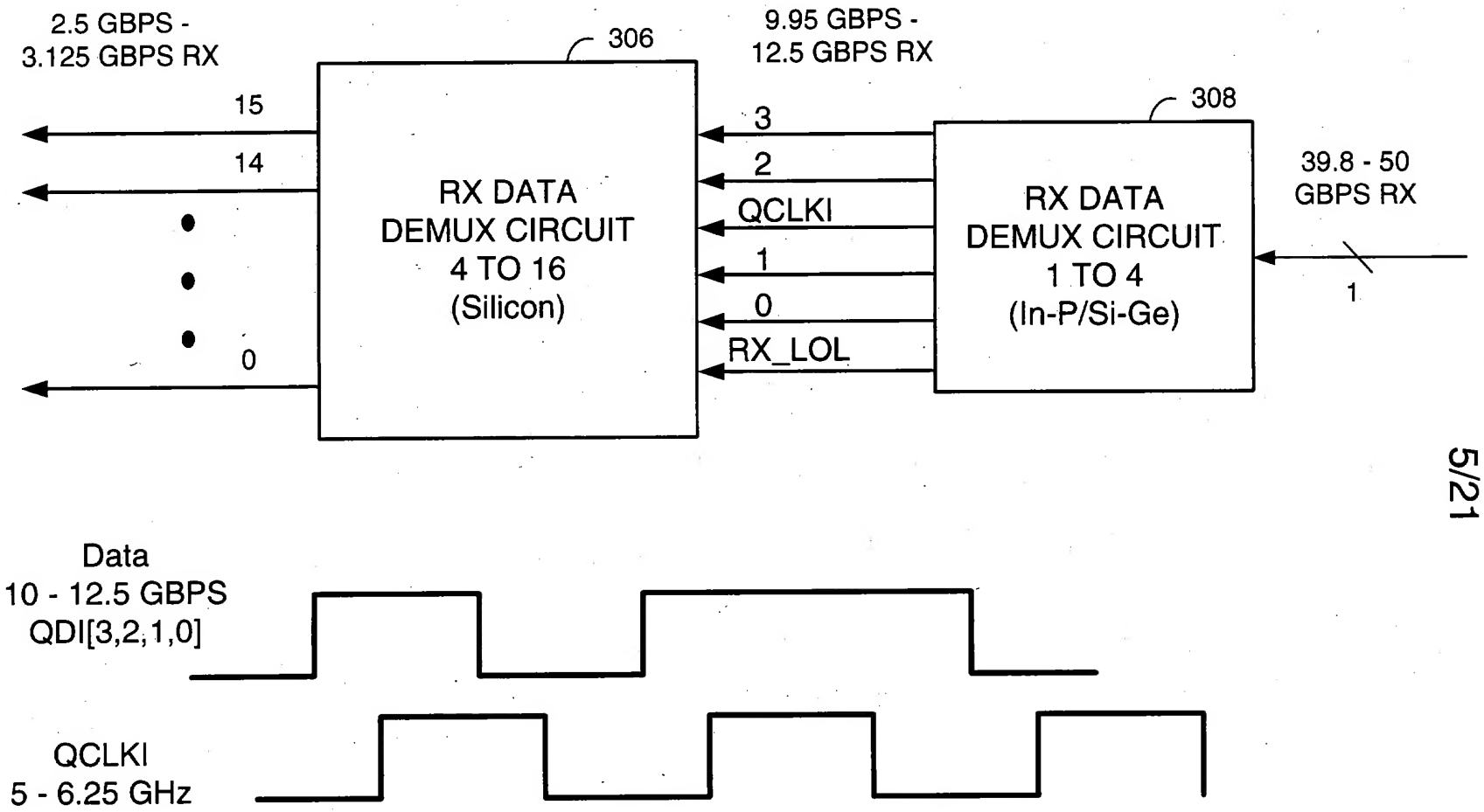
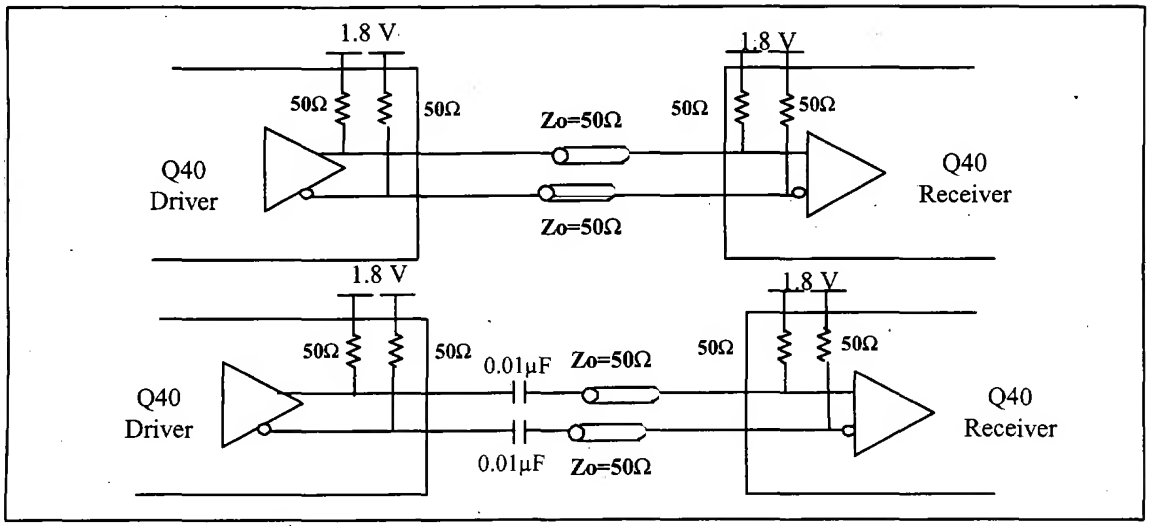

2.5 GBPS -
3.125 GBPS RX
306
9.95 GBPS -
12.5 GBPS RX
308
15
14
0
RX DATA
DEMUX CIRCUIT
4 TO 16
(Silicon)
3
2
QCLKI
1
0
RX_LOL
RX DATA
DEMUX CIRCUIT
1 TO 4
(In-P/Si-Ge)
39.8 - 50
GBPS RX
1
Data
10 - 12.5 GBPS
QDI[3,2,1,0]
QCLKI
5 - 6.25 GHz

FIG. 5

Receiver Input and Source Centered Clock Performance

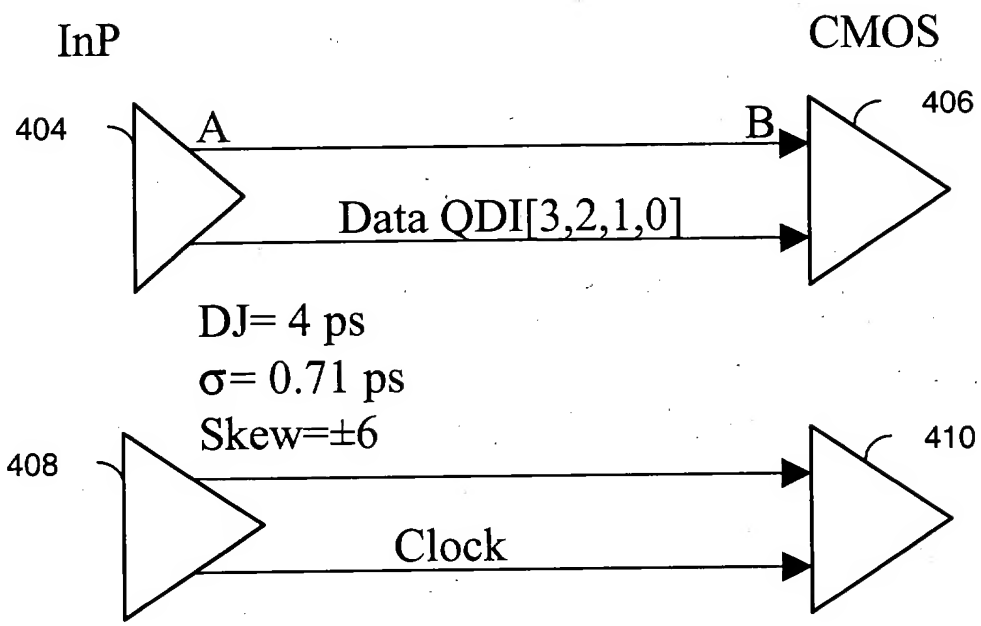
Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Output Common Mode	Vcm	See Figure Below	1575	1675	1775	mV
Single Ended Output Impedance	Z_{SE}		40	50	60	Ω
Differential Input impedance	Z_d		80	100	120	Ω
Input Impedance Mismatch	Z_M				10	%
Q40, CML Input Differential Amplitude, p-p	Δ VQDO	See Figure Below	400	500	600	mV
Q40 Input Rise and Fall Time (20% to 80%)	t_{RH} , t_{FH}			25	35	ps
Differential output return loss*	S11	Up to 7.5 GHz	10			dB
4-by-1 mux input return loss >15 db at 10 GHz						



400

402

FIG. 6



Additional Sources:
Crosstalk = 4 ps
PCB Mismatch = 4 ps

At B: Total Input Jitter = 4+4+12+4+4+4+0.71*14= 42 ps
CMOS Input Mismatch + setup/Hold = 24 ps
Margin at 10 Gig = 32 ps
Margin at 12.5 Gig = 12 ps

FIG. 7

Transmit and Receive

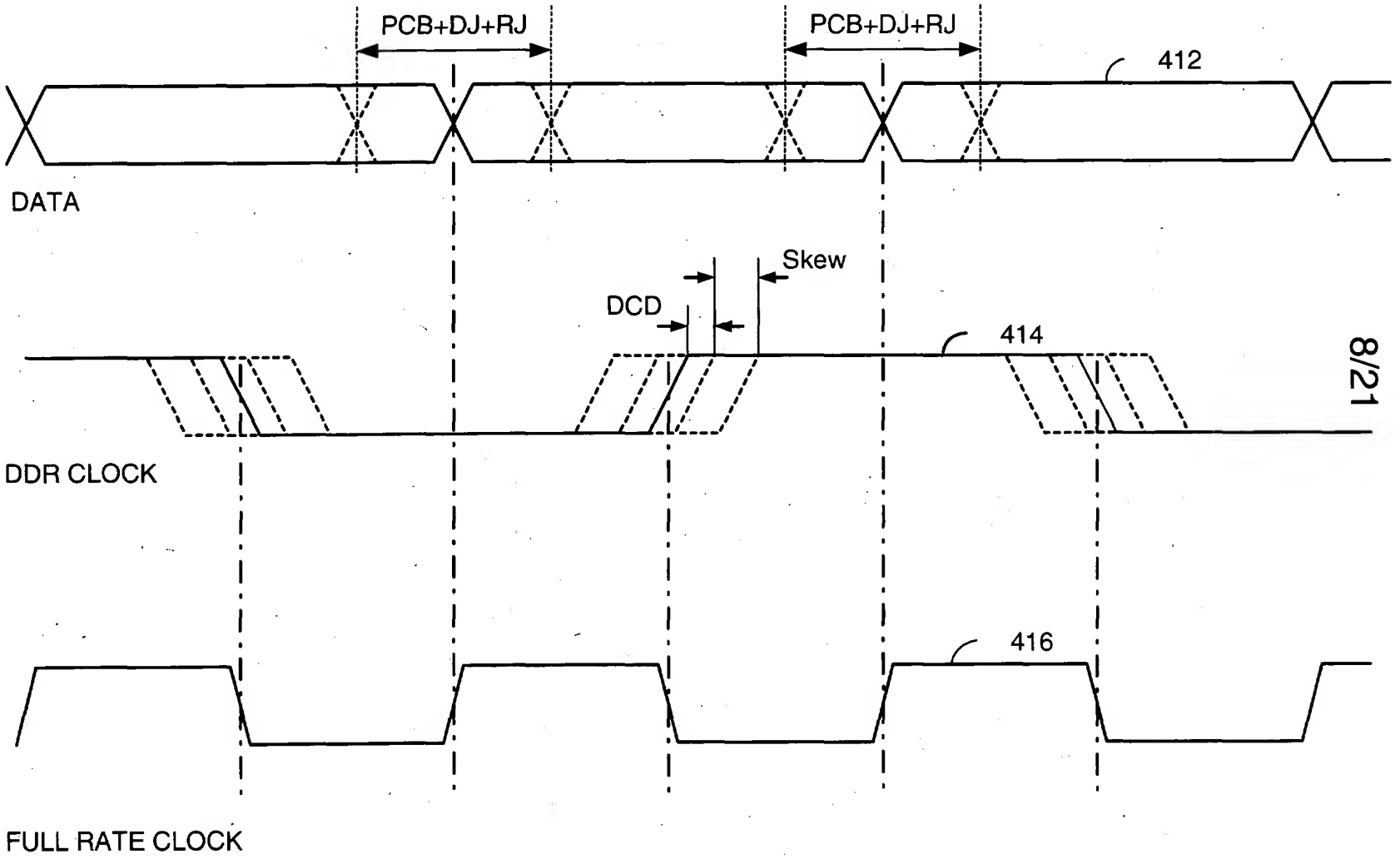


FIG. 8

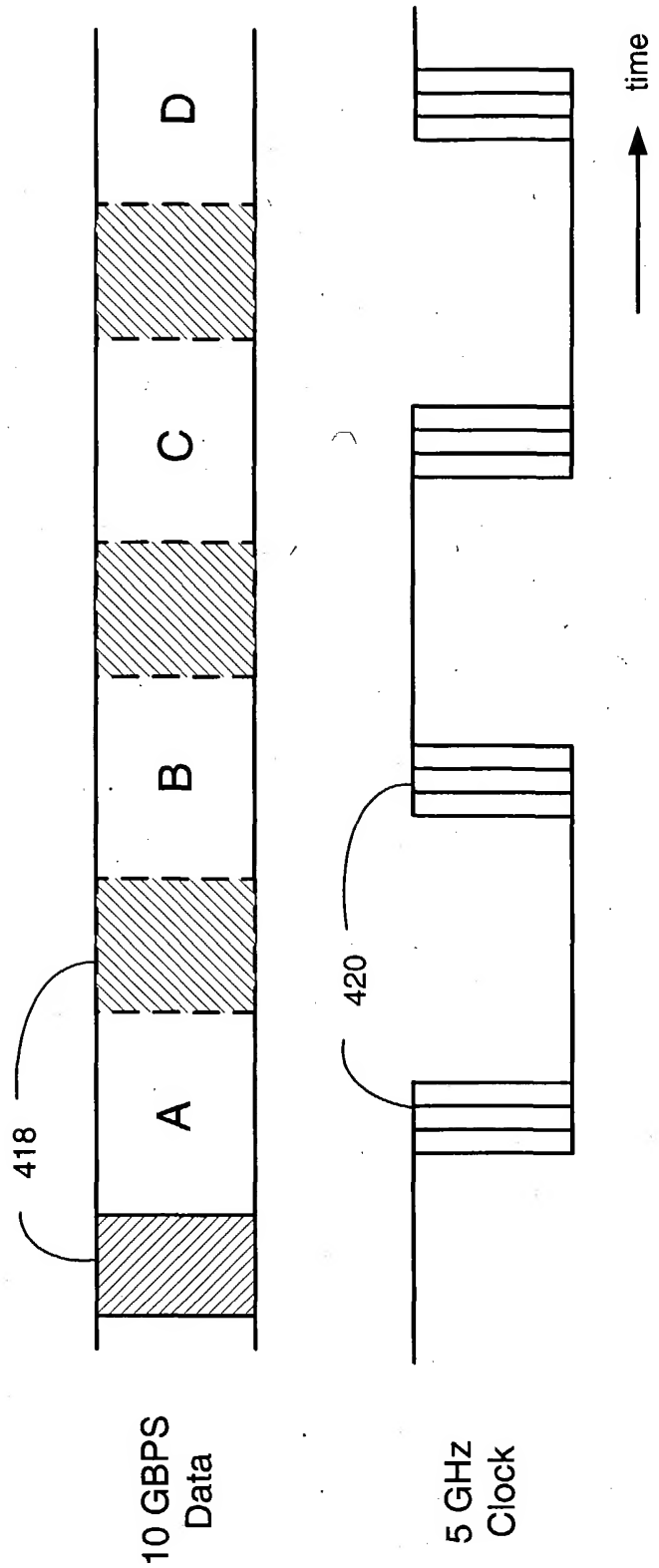


FIG. 9

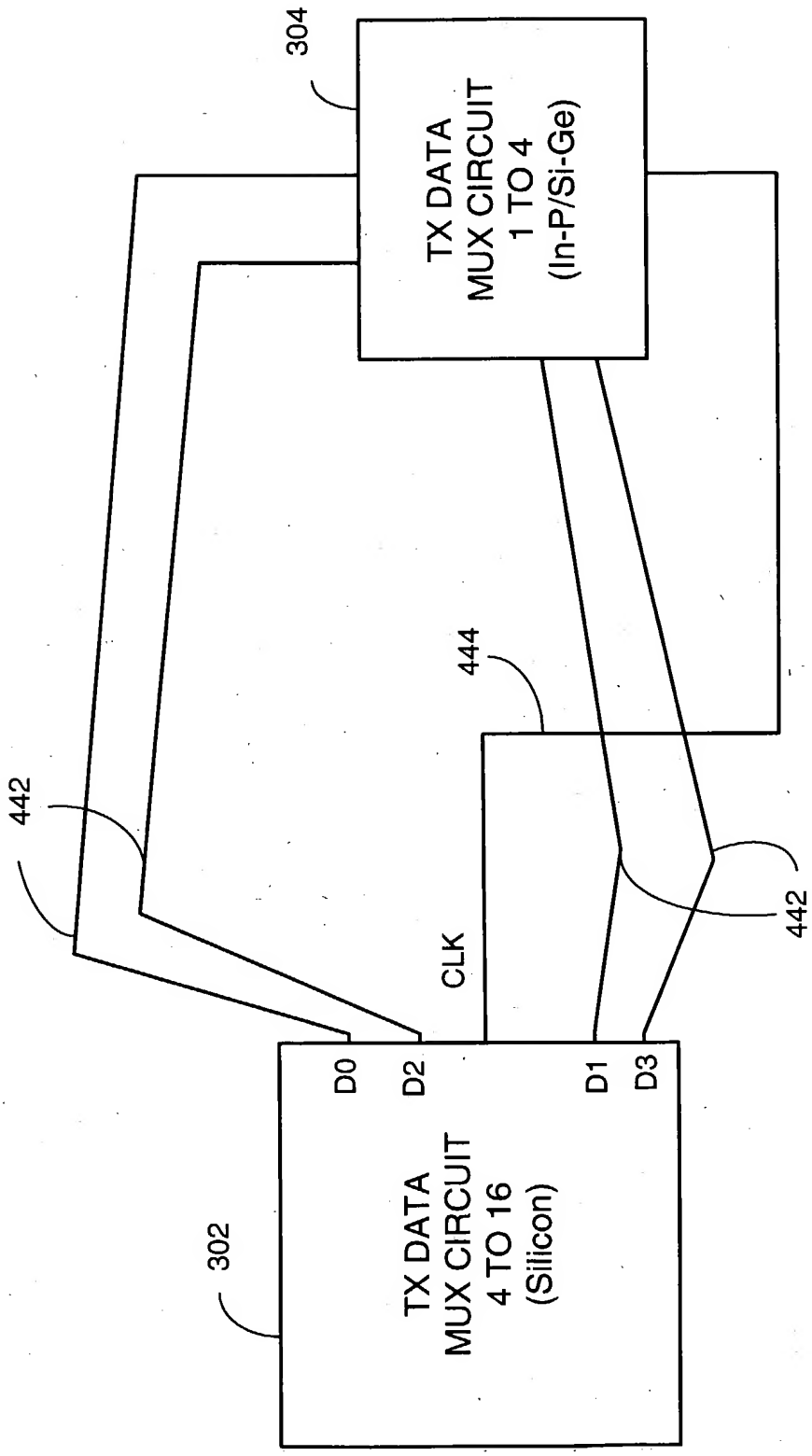

304
TX DATA
MUX CIRCUIT
1 TO 4
(In-P/Si-Ge)
442
444
442
CLK
D0
D2
D1
D3
302
TX DATA
MUX CIRCUIT
4 TO 16
(Silicon)

FIG. 10B

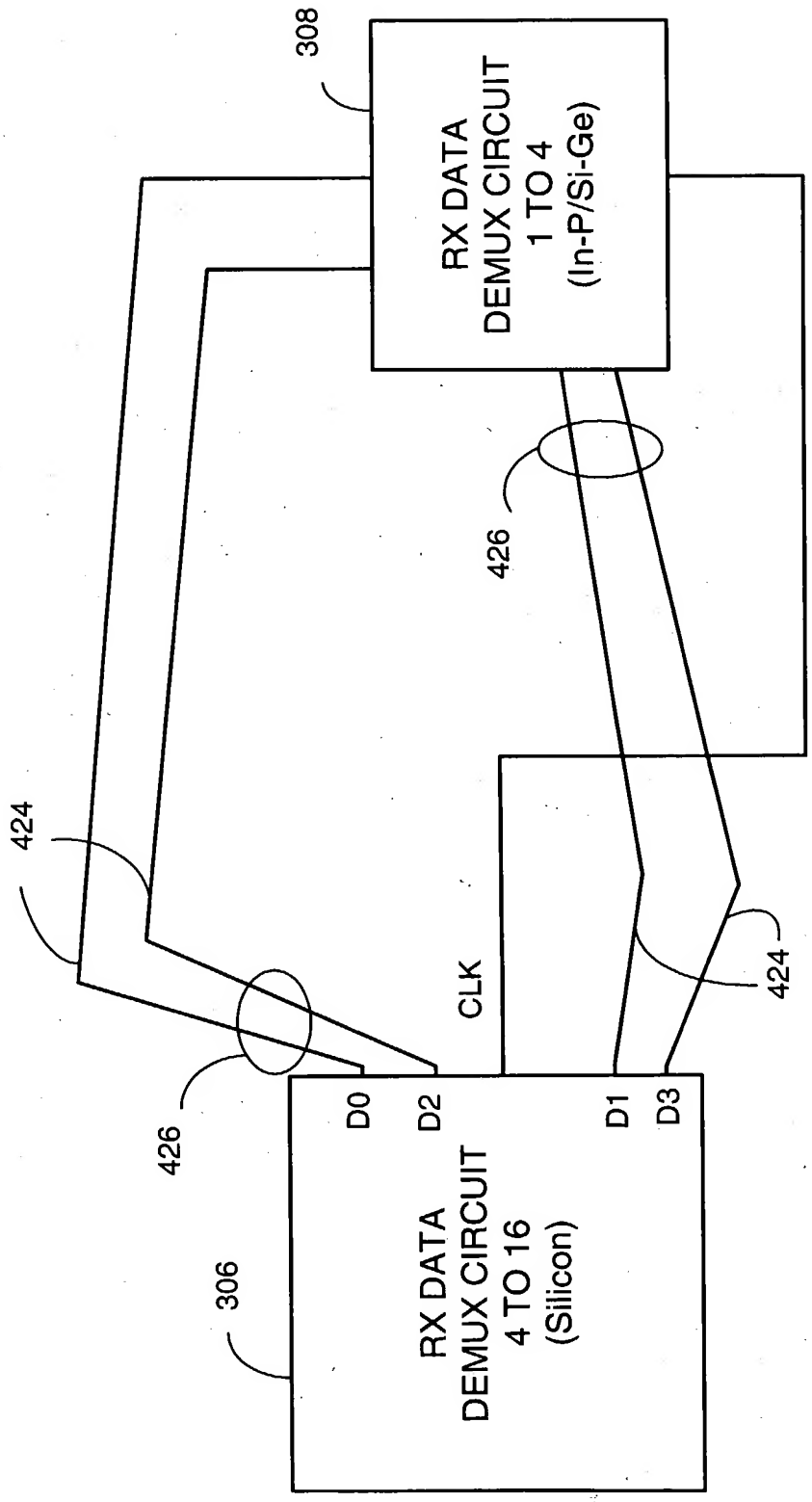

308
RX DATA
DEMUX CIRCUIT
1 TO 4
(In-P/Si-Ge)
426
424
CLK
424
426
D0
D2
D1
D3
306
RX DATA
DEMUX CIRCUIT
4 TO 16
(Silicon)

FIG. 10A

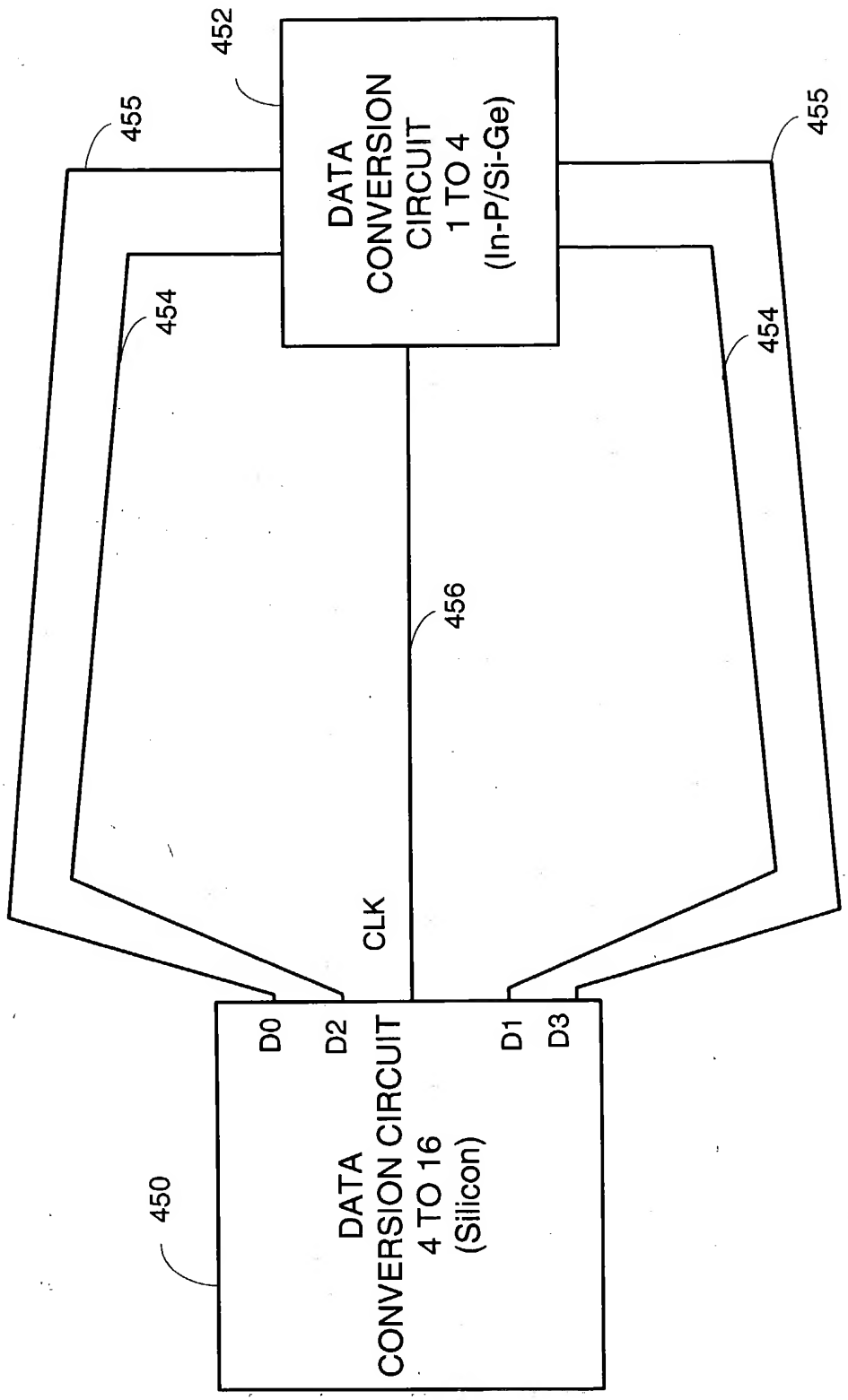

452
DATA
CONVERSION
CIRCUIT
1 TO 4
(In-P/Si-Ge)
455
455
454
454
456
CLK
D0
D2
D1
D3
DATA
CONVERSION CIRCUIT
4 TO 16
(Silicon)
450

FIG. 10C

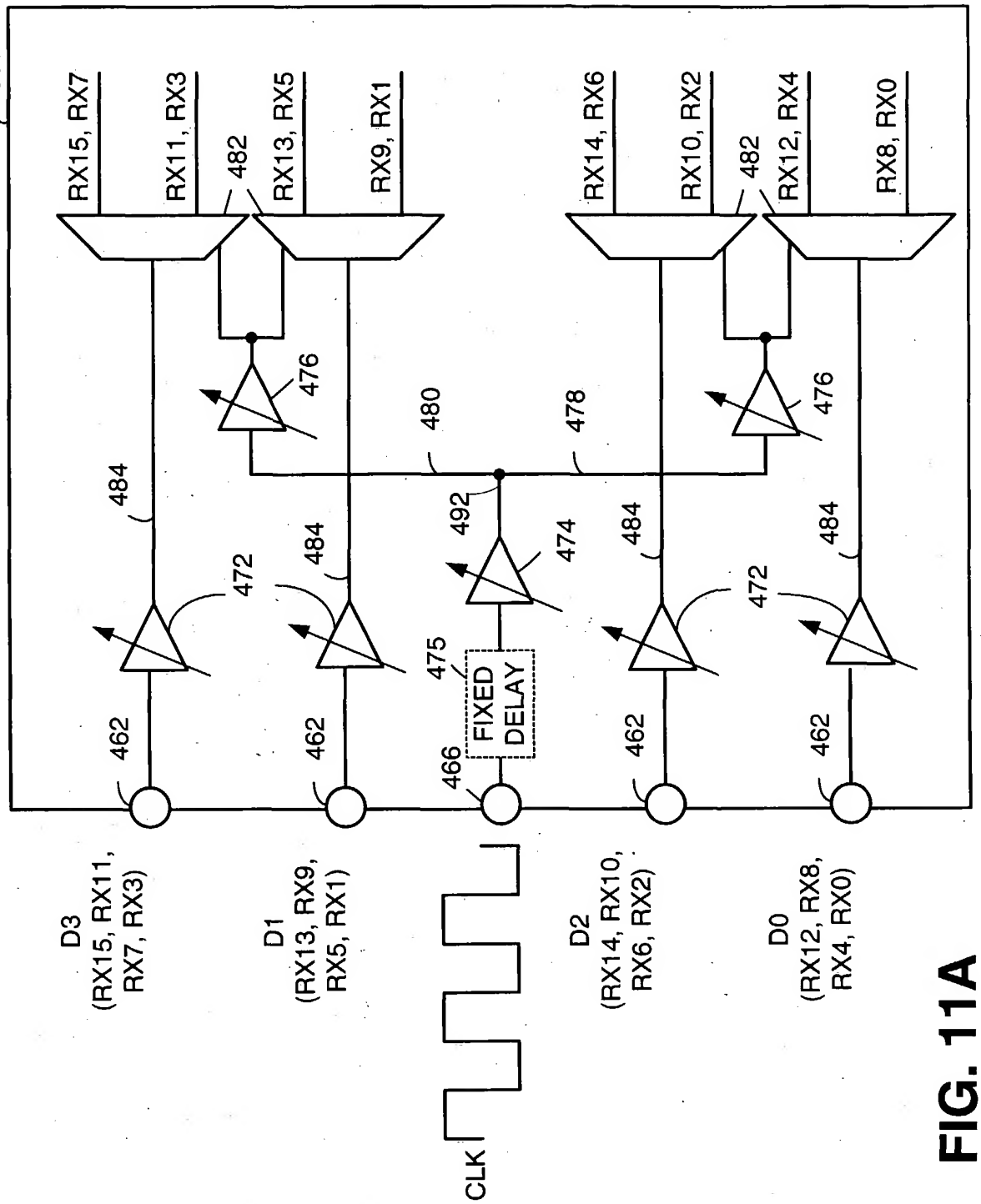

306
RX15, RX7
RX11, RX3
482
RX13, RX5
RX9, RX1
RX14, RX6
RX10, RX2
482
RX12, RX4
RX8, RX0
476
476
480
478
484
484
484
484
492
474
472
472
475
FIXED DELAY
462
462
466
462
462
D3 (RX15, RX11, RX7, RX3)
D1 (RX13, RX9, RX5, RX1)
D2 (RX14, RX10, RX6, RX2)
D0 (RX12, RX8, RX4, RX0)
CLK

FIG. 11A

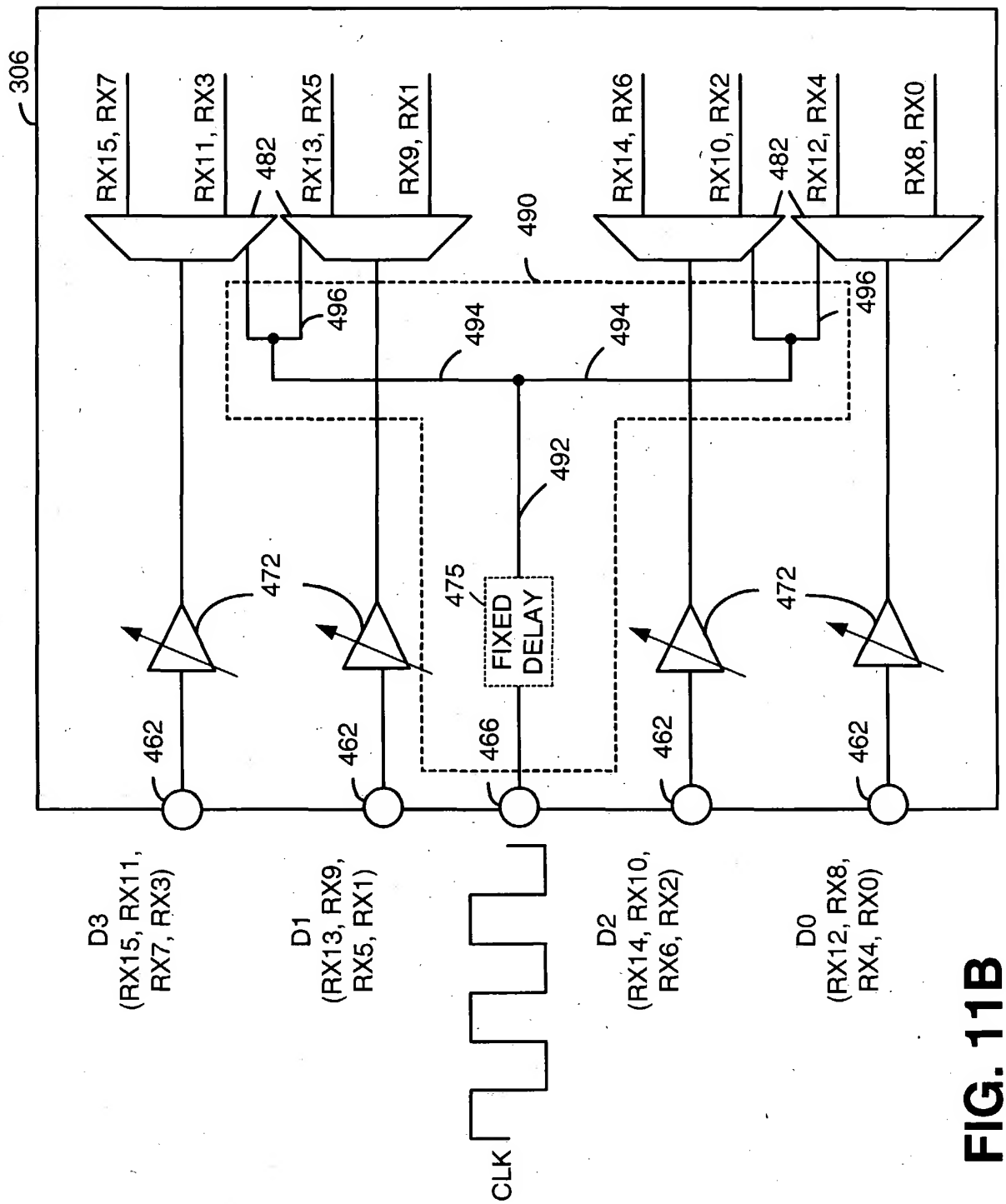

306
RX15, RX7
RX11, RX3
482
RX13, RX5
RX9, RX1
490
RX14, RX6
RX10, RX2
482
RX12, RX4
RX8, RX0
496
494
494
496
492
475
FIXED DELAY
472
472
462
462
466
462
462
D3 (RX15, RX11, RX7, RX3)
D1 (RX13, RX9, RX5, RX1)
D2 (RX14, RX10, RX6, RX2)
D0 (RX12, RX8, RX4, RX0)
CLK

FIG. 11B

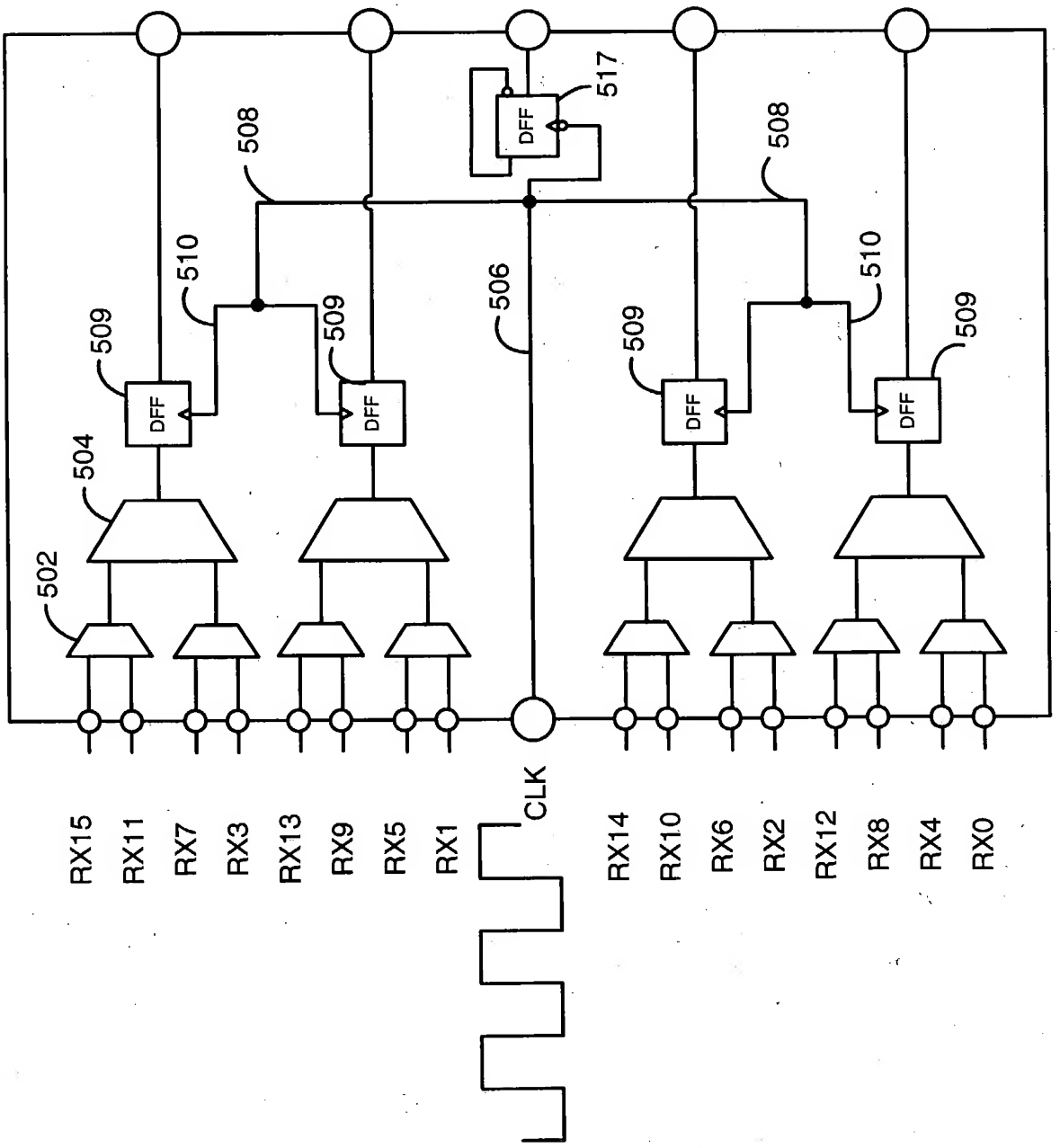

D3
(RX15, RX11,
RX7, RX3)
D1
(RX13, RX9,
RX5, RX1)
D2
(RX14, RX10,
RX6, RX2)
D0
(RX12, RX8,
RX4, RX0)
502
504
509
510
508
506
517
DFF
CLK
RX15
RX11
RX7
RX3
RX13
RX9
RX5
RX1
RX14
RX10
RX6
RX2
RX12
RX8
RX4
RX0

FIG. 11C

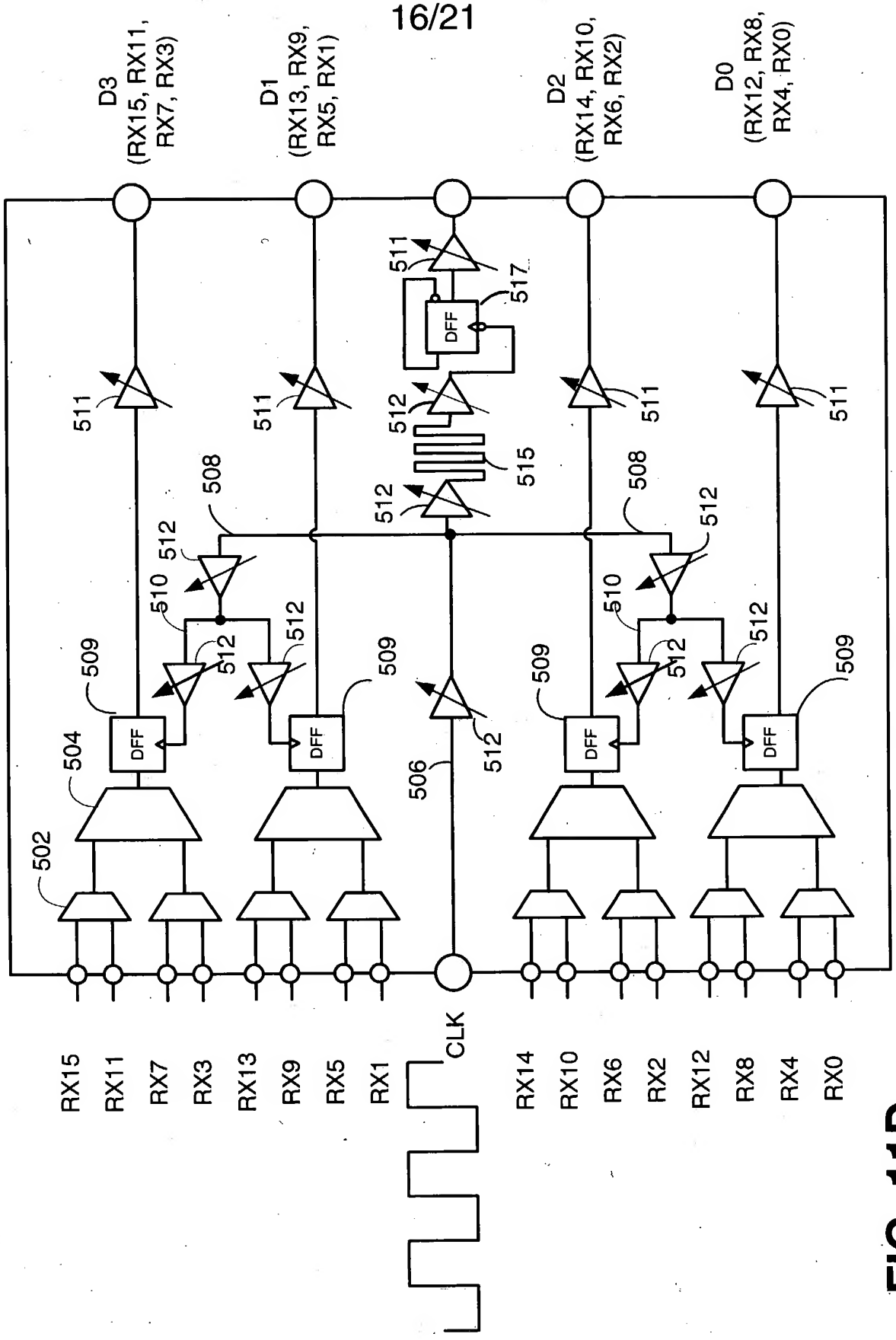

D3
(RX15, RX11,
RX7, RX3)
D1
(RX13, RX9,
RX5, RX1)
D2
(RX14, RX10,
RX6, RX2)
D0
(RX12, RX8,
RX4, RX0)
511
508
512
510
509
504
502
506
515
517
DFF
CLK
RX15
RX11
RX7
RX3
RX13
RX9
RX5
RX1
RX14
RX10
RX6
RX2
RX12
RX8
RX4
RX0

FIG. 11D

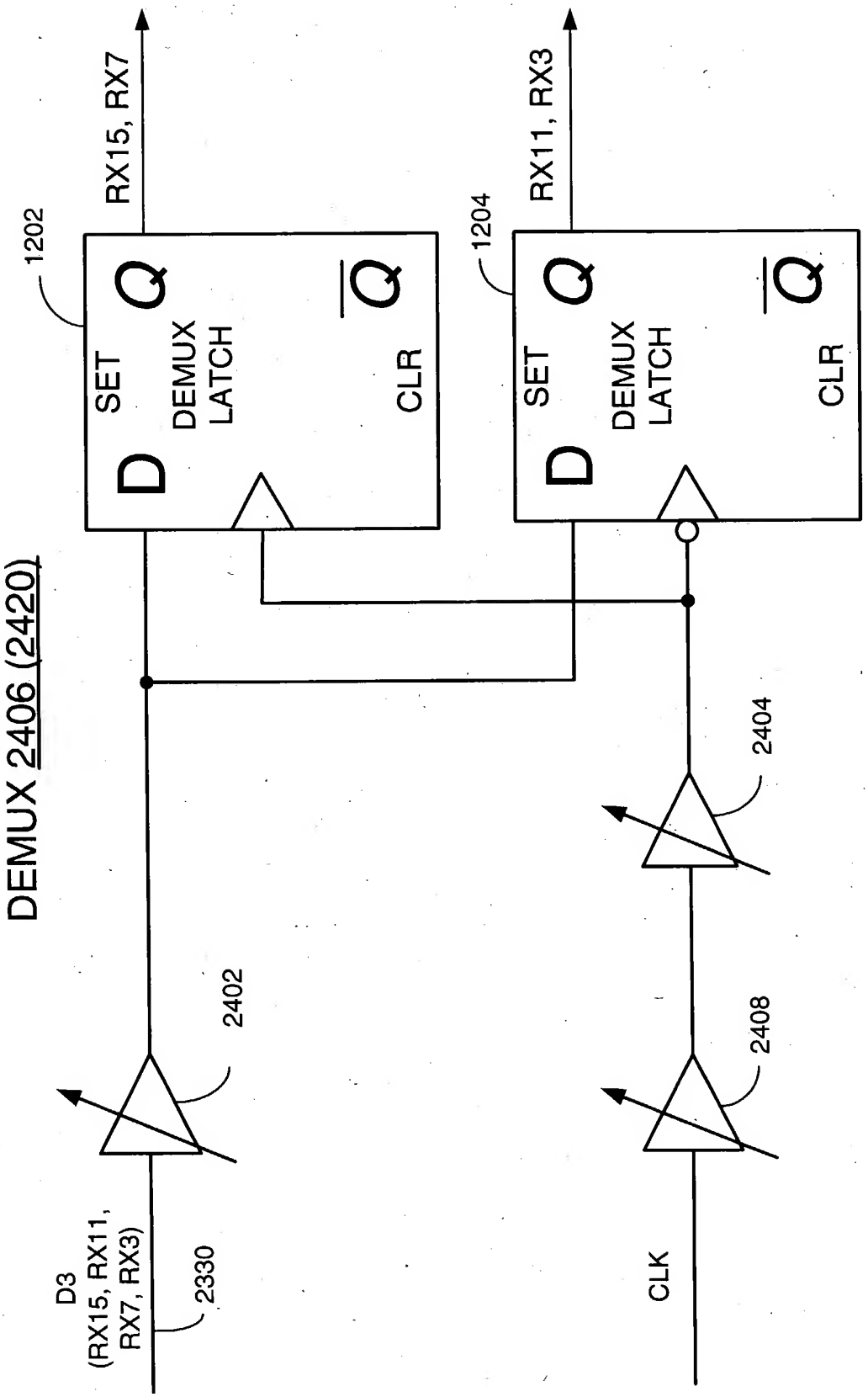

DEMUX 2406 (2420)
1202
RX15, RX7
SET
D
DEMUX LATCH
Q
CLR
Q
1204
RX11, RX3
SET
D
DEMUX LATCH
Q
CLR
Q
2402
2404
2408
D3
(RX15, RX11, RX7, RX3)
2330
CLK

FIG. 12A

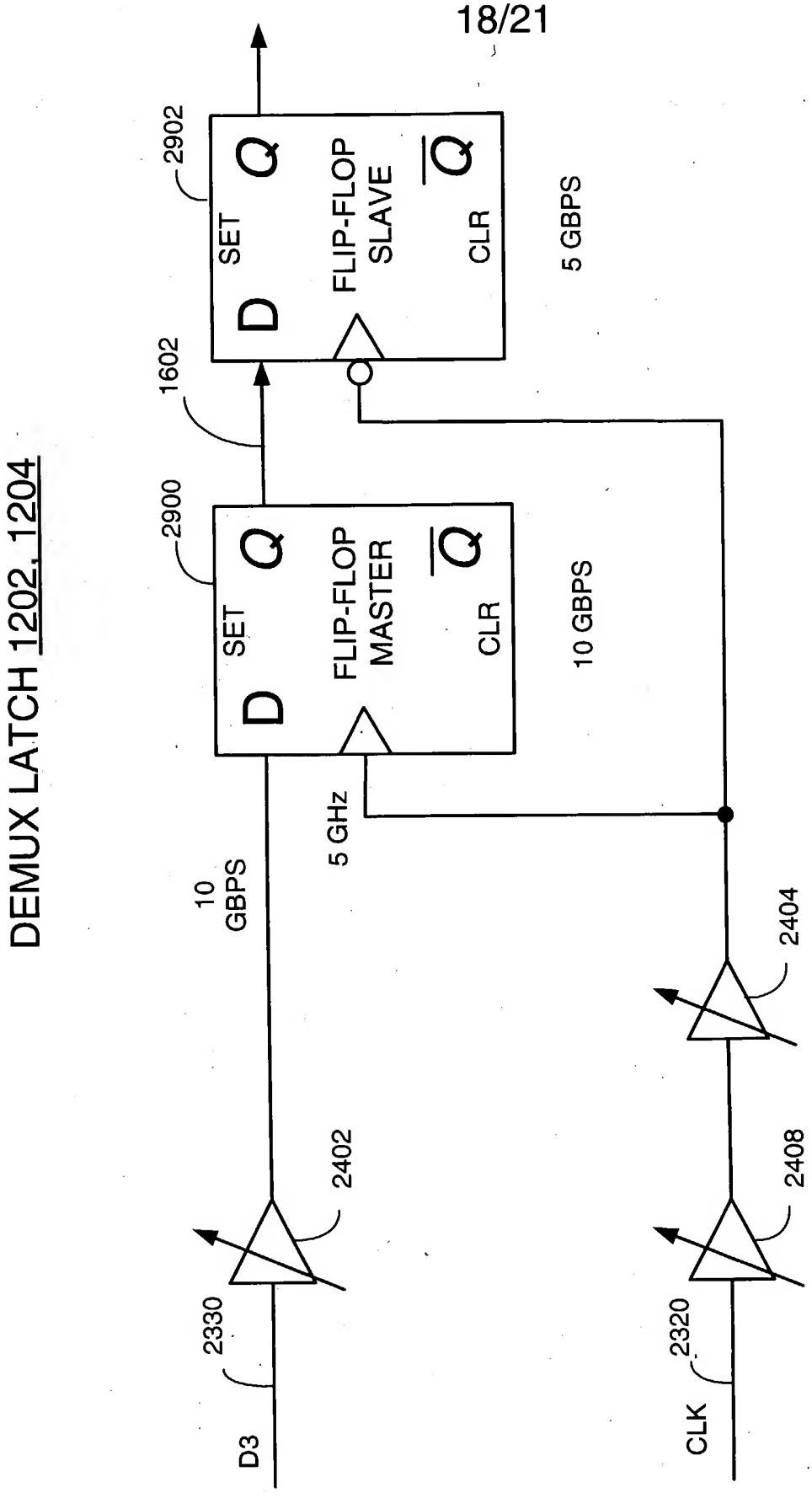

DEMUX LATCH 1202, 1204
2902
SET
Q
D
FLIP-FLOP
SLAVE
CLR
Q
5 GBPS
1602
2900
SET
Q
D
FLIP-FLOP
MASTER
CLR
Q
10 GBPS
10
GBPS
5 GHz
2404
2402
2408
2330
2320
D3
CLK

FIG. 12B

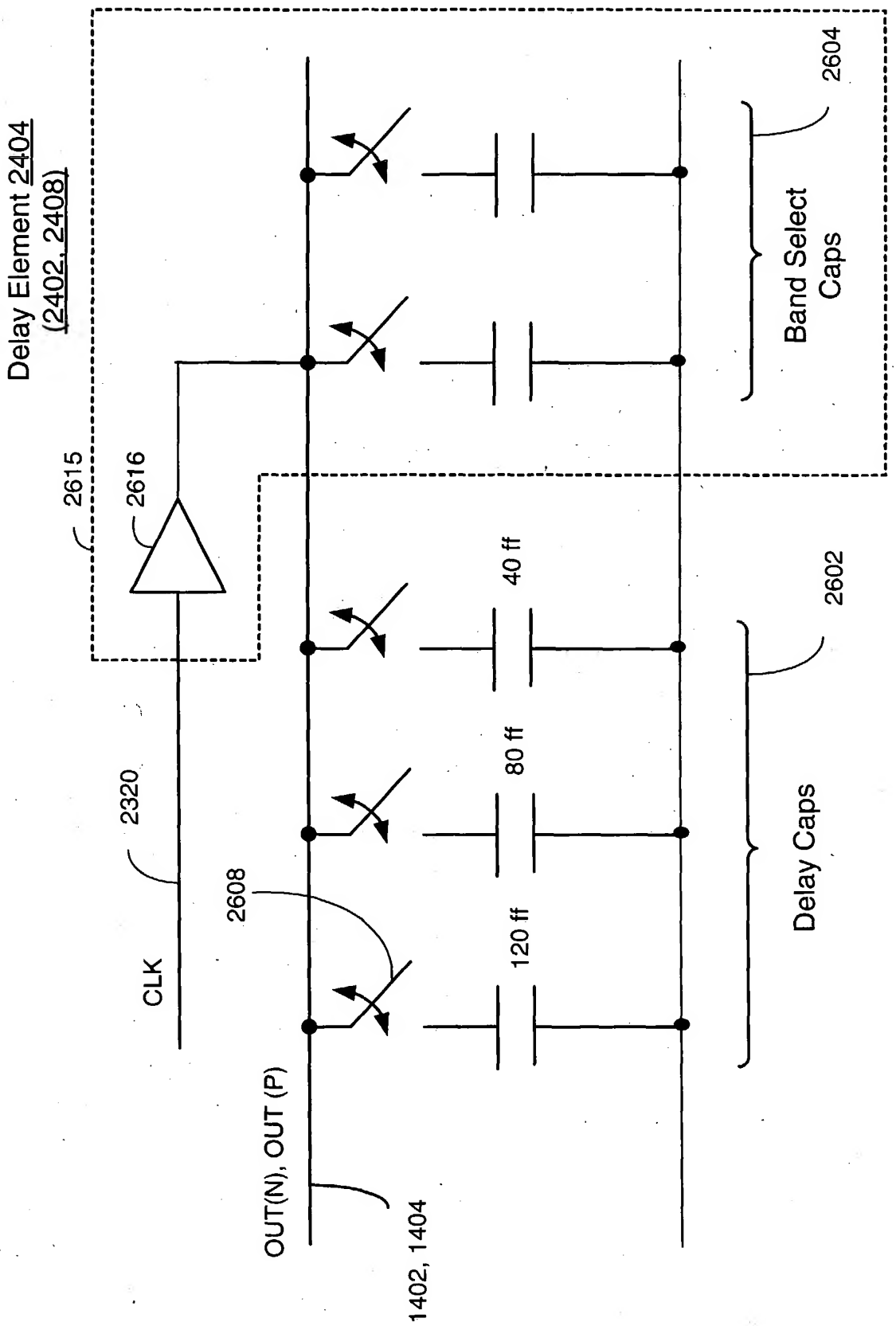

Delay Element 2404
(2402, 2408)
2615
2616
2320
CLK
2608
OUT(N), OUT (P)
1402, 1404
120 ff
80 ff
40 ff
Delay Caps
2602
Band Select
Caps
2604

FIG. 13

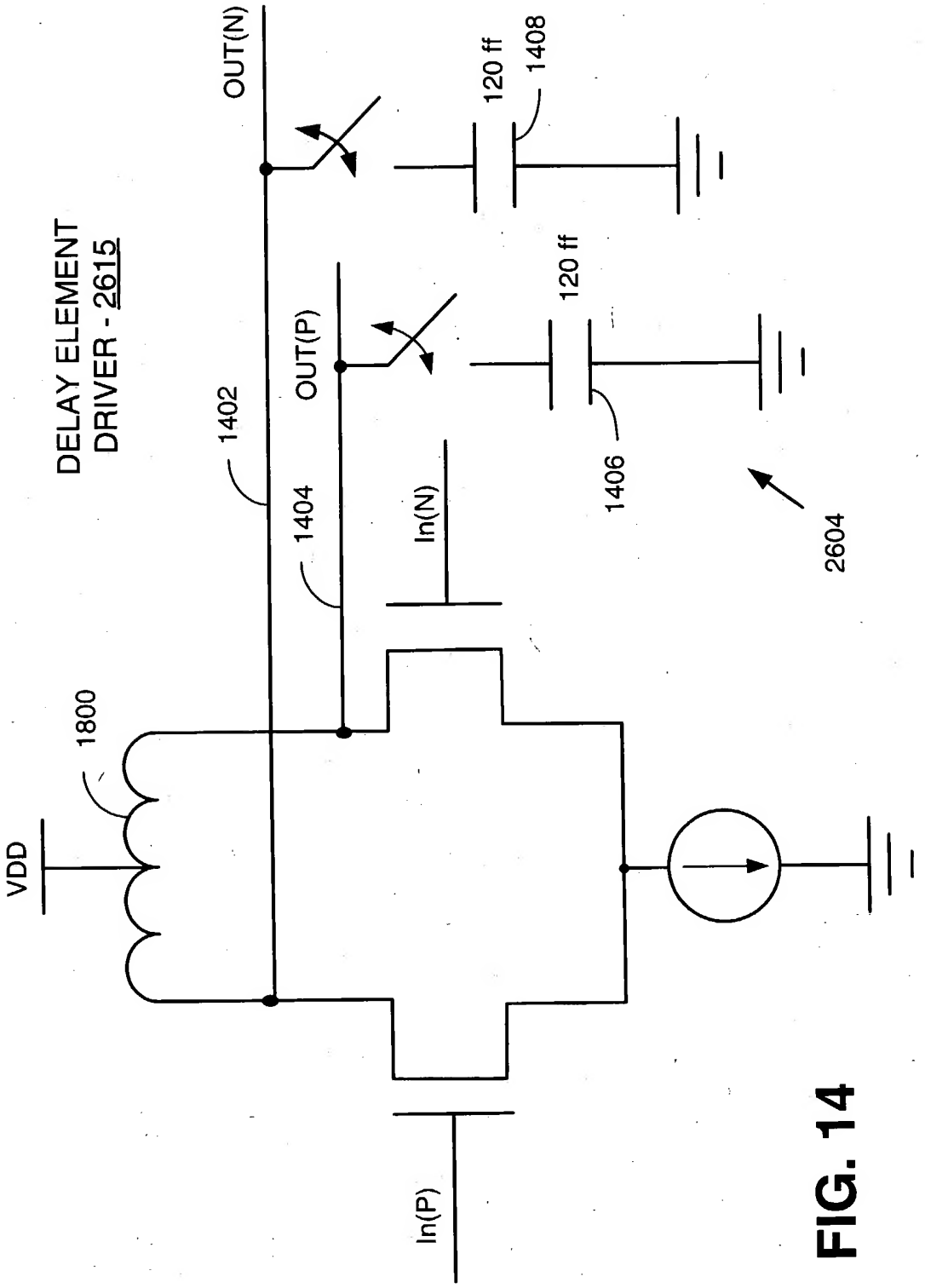

DELAY ELEMENT
DRIVER - 2615
VDD
1800
1402
1404
OUT(N)
OUT(P)
In(N)
In(P)
120 ff
1408
120 ff
1406
2604

FIG. 14

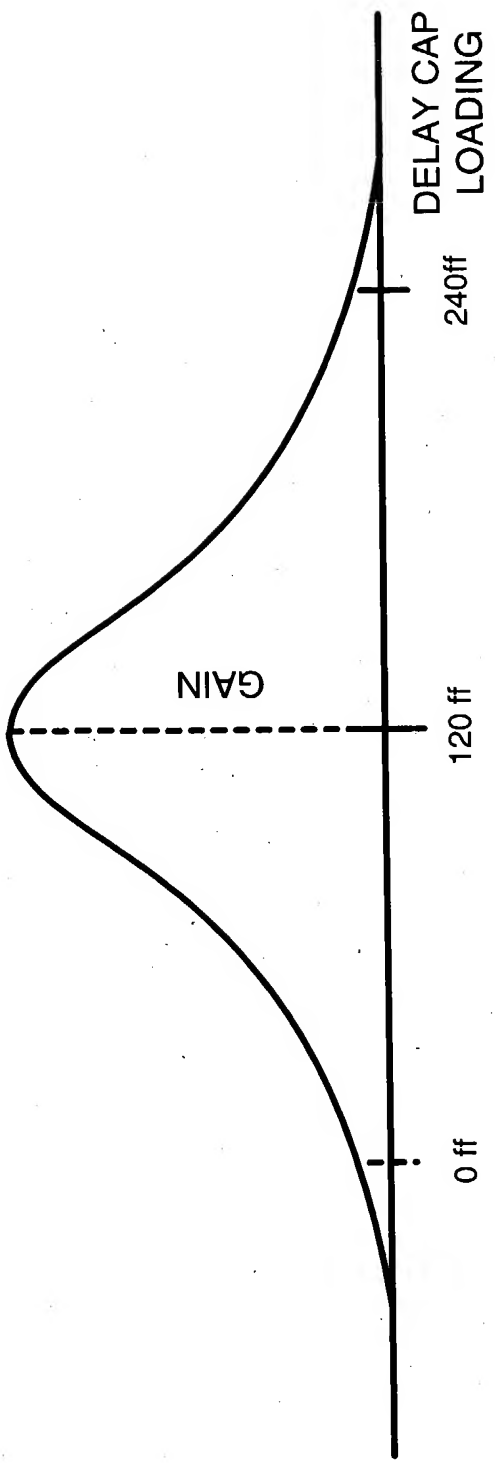


FIG. 15A

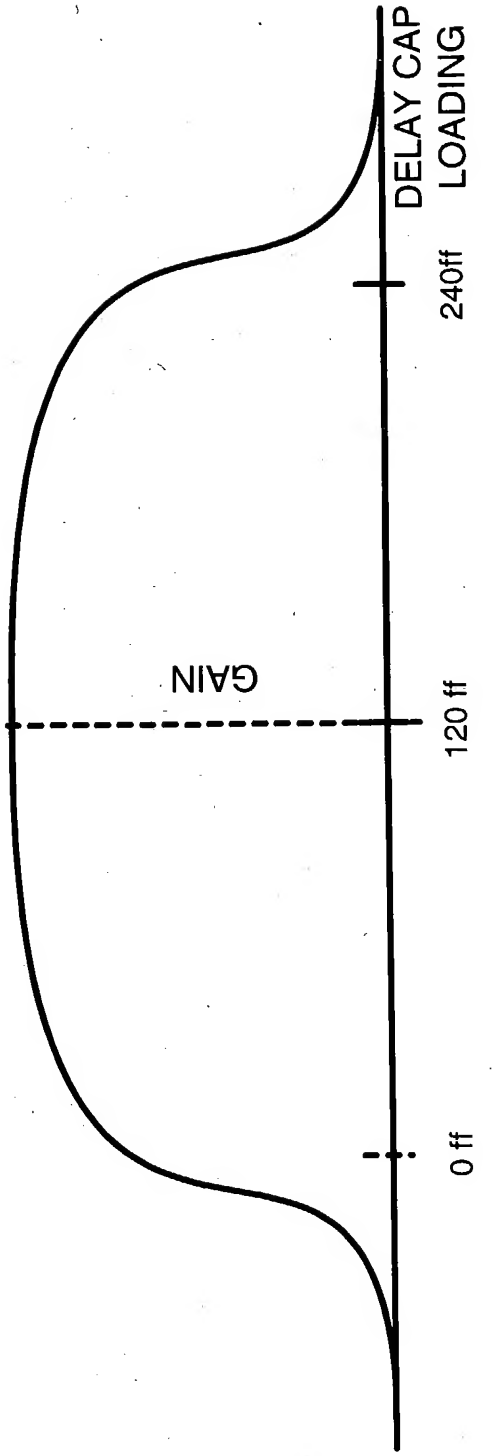


FIG. 15B